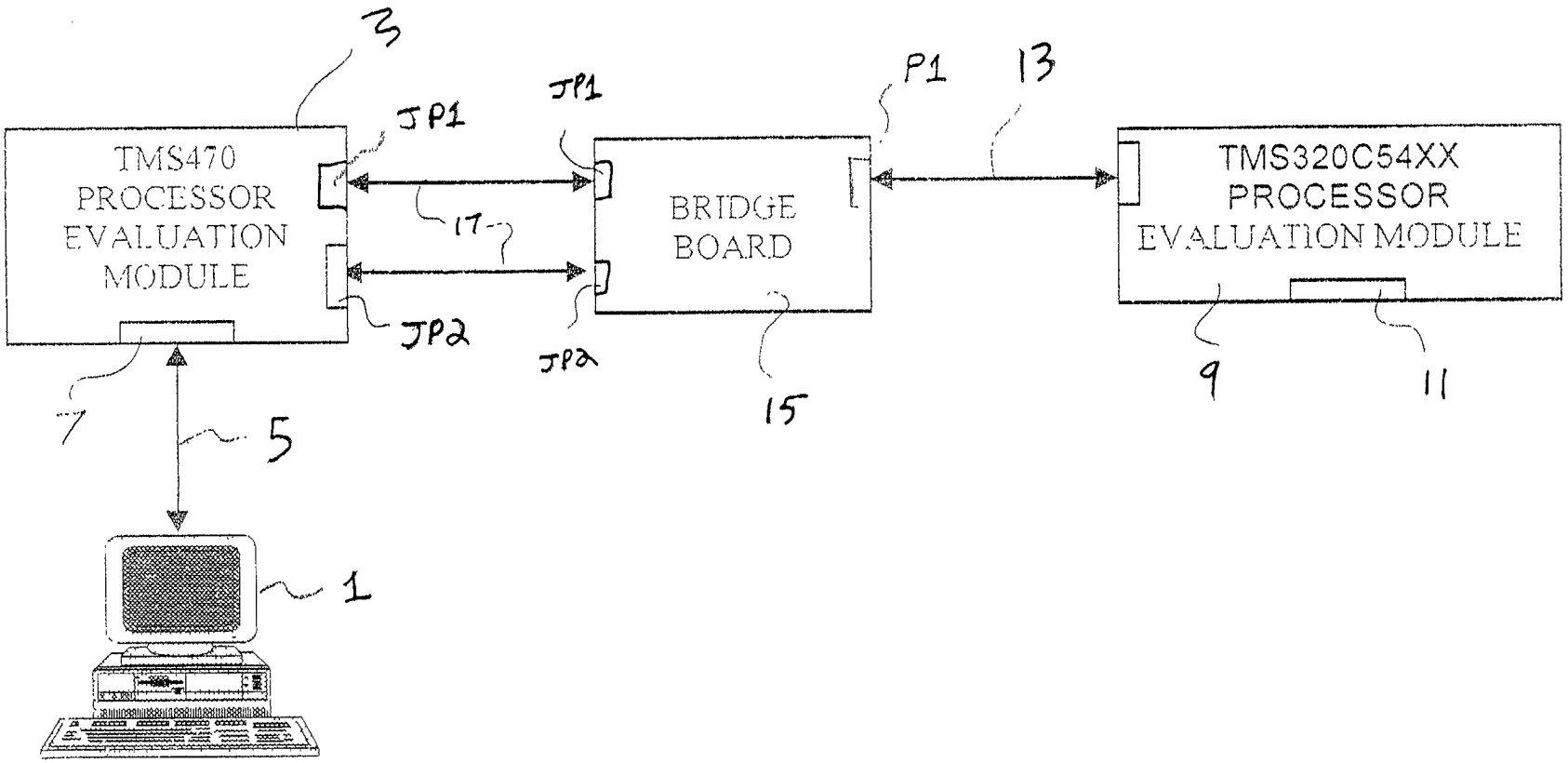
3
JP1
JP1
P1
13
TMS470
PROCESSOR
EVALUATION
MODULE
17
BRIDGE
BOARD
TMS320C54XX
PROCESSOR
EVALUATION MODULE
JP2
JP2
7
5
15
9
11
1

FIG. 1

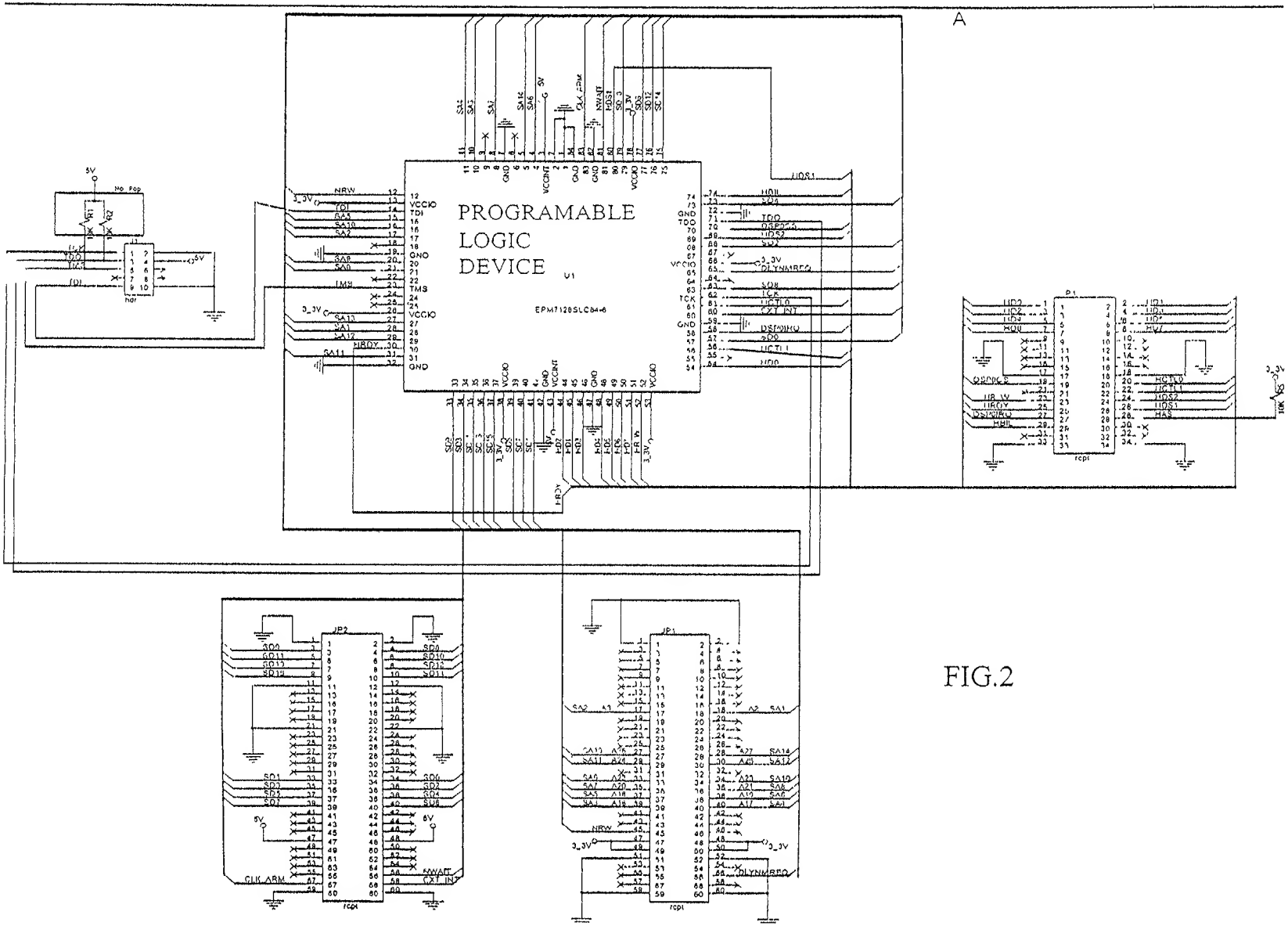

FIG.2

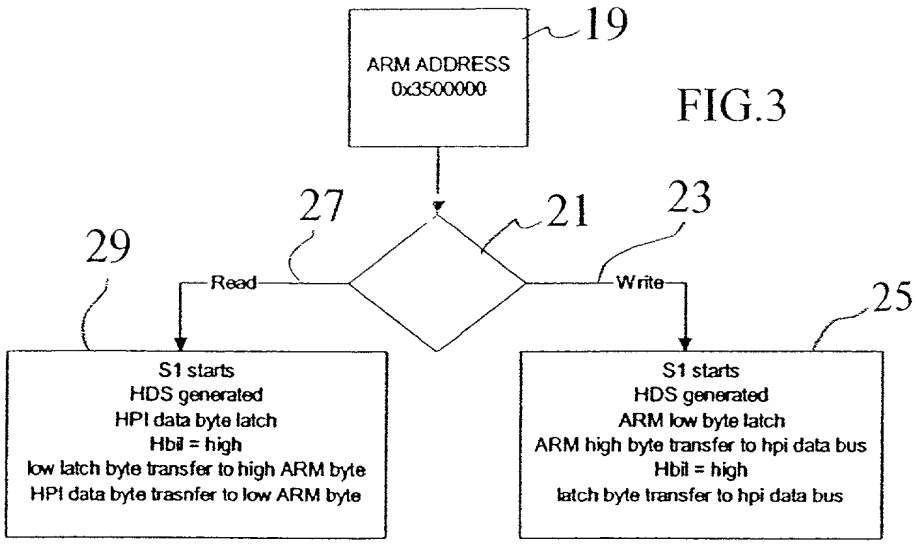
ARM ADDRESS
0x3500000
19
27
21
23
29
Read
Write
25
S1 starts
HDS generated
HPI data byte latch
Hbil = high
low latch byte transfer to high ARM byte
HPI data byte trasnfer to low ARM byte
S1 starts
HDS generated
ARM low byte latch
ARM high byte transfer to hpi data bus
Hbil = high
latch byte transfer to hpi data bus

FIG.3

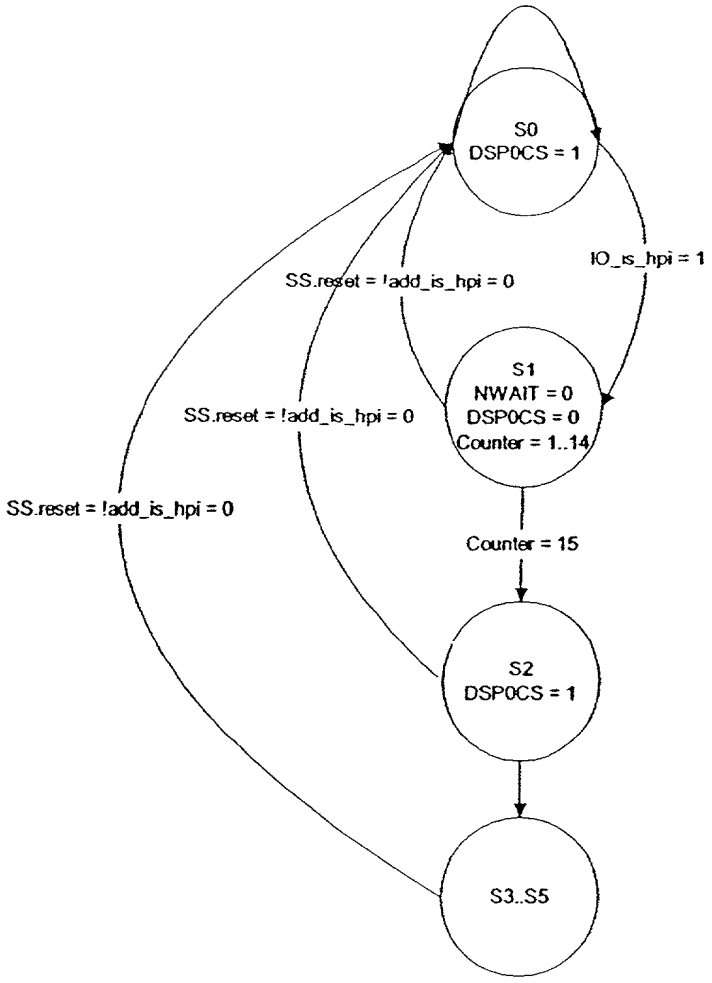
S0
DSP0CS = 1
IO_is_hpi = 1
SS.reset = !add_is_hpi = 0
S1
NWAIT = 0
DSP0CS = 0
Counter = 1..14
SS.reset = !add_is_hpi = 0
SS.reset = !add_is_hpi = 0
Counter = 15
S2
DSP0CS = 1
S3..S5

FIG.4

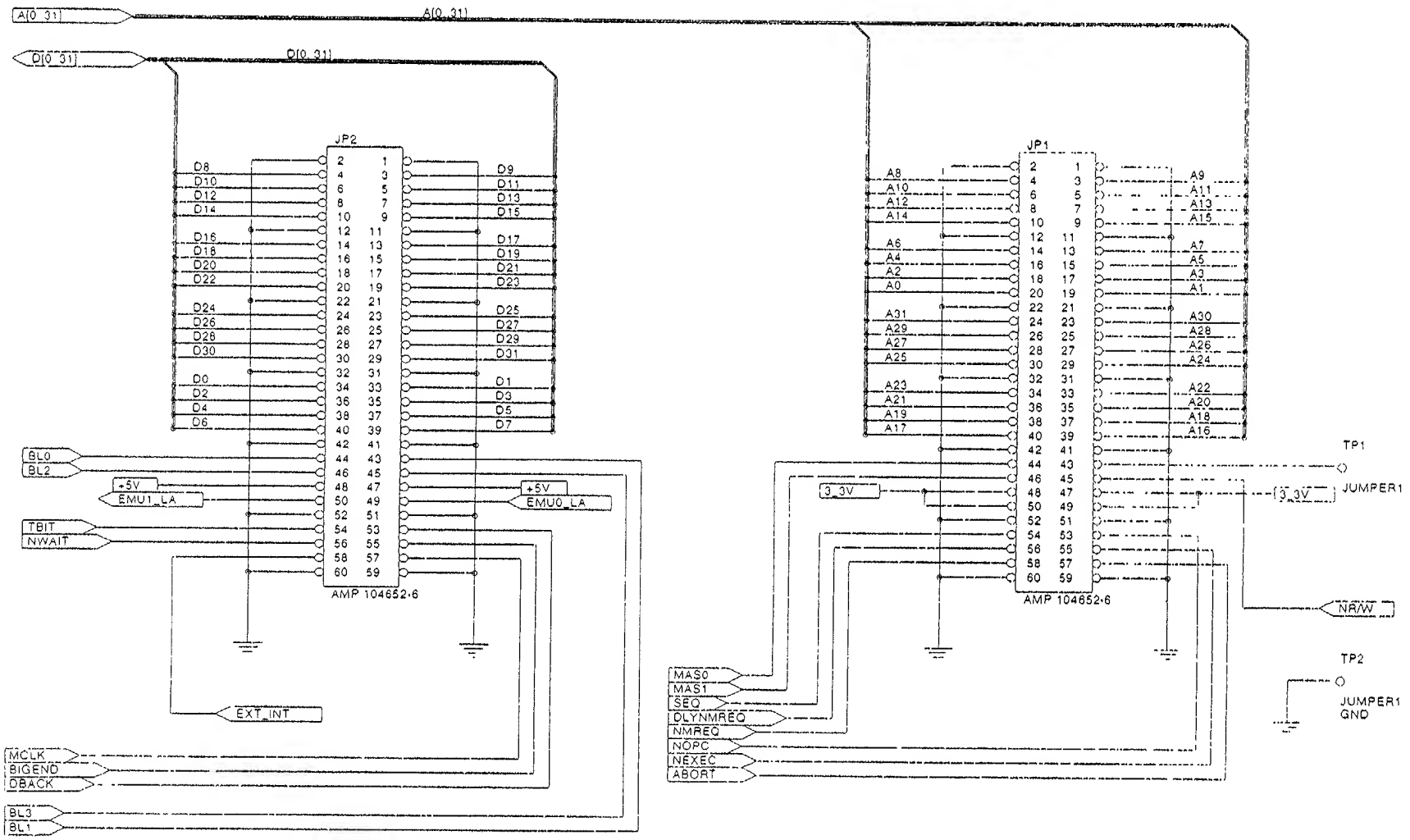
A[0..31]
D[0..31]
JP2
AMP 104652-6
JP1
AMP 104652-6
BL0
BL2
+5V
EMU1_LA
+5V
EMU0_LA
TBIT
NWAIT
EXT_INT
MCLK
BIGEND
DBACK
BL3
BL1
3.3V
3.3V
JUMPER1
TP1
NR/W
TP2
JUMPER1
GND
MAS0
MAS1
SEQ
DLYNMREQ
NMREQ
NOPC
NEXEC
ABORT

FIG.5

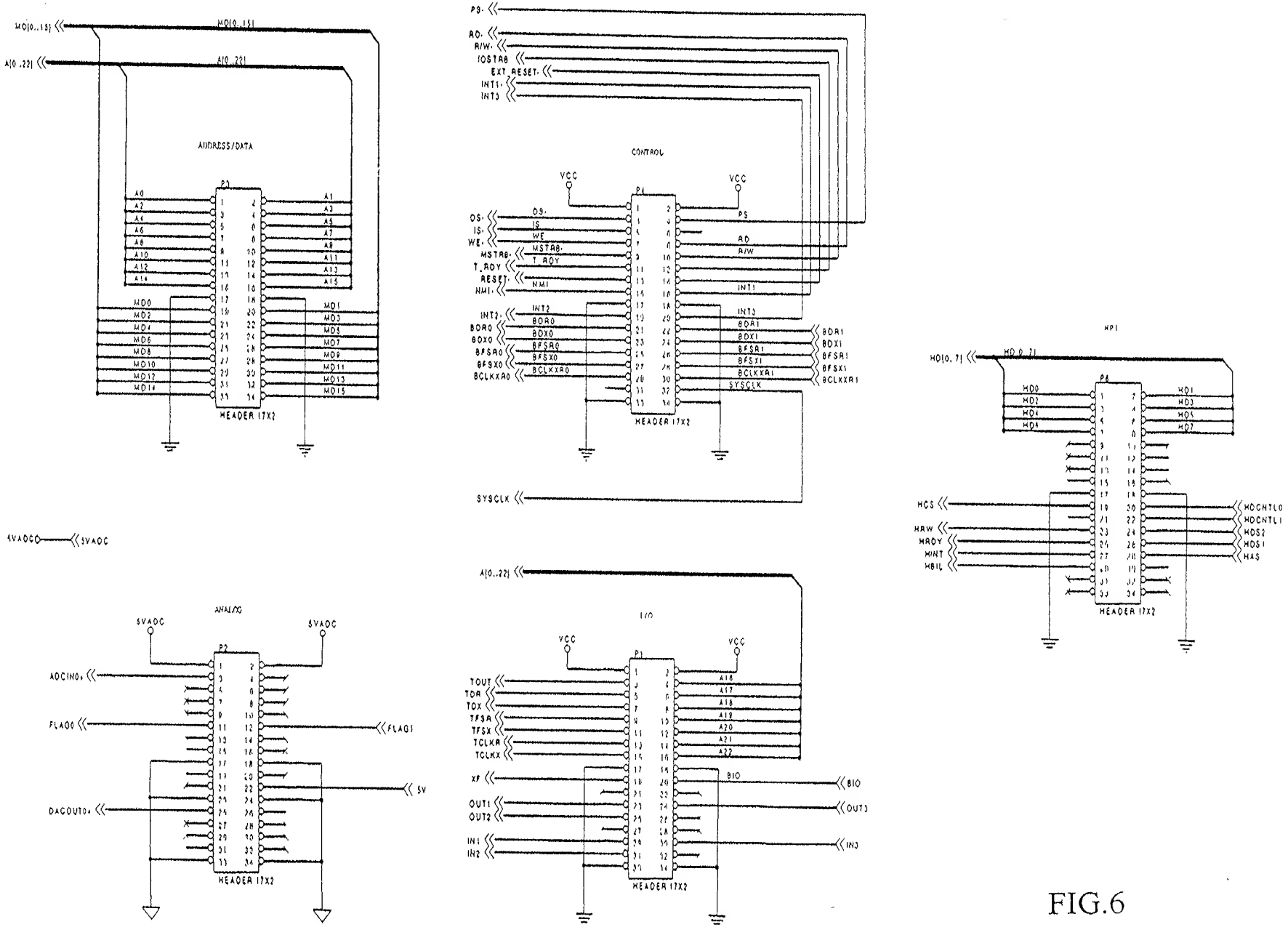
MD[0..15]
A[0..22]
ADDRESS/DATA
P3
HEADER 17X2
P9
RD
R/W
IOSTRB
EXT_RESET
INT1
INT3
CONTROL
VCC
P1
OS
IS
WE
MSTRB
T_RDY
RESET
NMI
INT2
BDR0
BDX0
BFSR0
BFSX0
BCLKXR0
BDR1
BDX1
BFSR1
BFSX1
BCLKXR1
SYSCLK
HPI
HD[0..7]
P4
HCS
HRW
HRDY
HINT
HBIL
HDCNTL0
HDCNTL1
HDS2
HDS1
HAS
SVADC
ANALOG
P2
AOCIN0
FLAG0
FLAG1
5V
DACOUT0
I/O
TOUT
TDR
TOX
TFSR
TFSX
TCLKR
TCLKX
XF
OUT1
OUT2
IN1
IN2
BIO
OUT3
IN3

FIG.6